REMARKS

Claims 1, 3-7, 9, 16-20, 22-26, 28, 35-39, 42, 44, 51-55, 57-61, 63, 70-74, 76-80, 82, 89-92, and 98 are pending after amendment, with claims 1, 20, 39, 55, and 74 being independent. Claims 1, 20, 39, 42, 55, and 74 have been amended. Claims 2, 8, 10-15, 21, 27, 29-34, 40-41, 43, 45-50, 56, 62, 64-69, 75, 81, 83-88, and 93-97 have been cancelled. Claim 98 has been added. No new matter has been added.

In light of the foregoing amendment and following remarks, reconsideration and allowance of all pending claims are respectfully requested.

Rejection Under 35 U.S.C. § 103

Claim 39 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over US Patent No. 6,781,474 to Douziech et al. ("Douziech") in view of US Patent No. 5,963,856 to Kim ("Kim). While not agreeing with the rejections, claim 39 has been amended to obviate the rejection.

Claim 39 has been amended to recite "[a] method for calibrating a filter circuit, the filter circuit receiving an input signal and producing a filtered output signal, the method comprising: initializing a digital component code corresponding to switches associated with capacitive components in the filter circuit to a value such that an initial peak frequency of the filter circuit is below or above a desired frequency; initializing a digital gain code to a value such that a modified filtered output signal produced by a variable gain stage is greater than a DC reference voltage, wherein the variable gain stage is modifying the filtered output signal based on the initialized digital gain code; producing an amplitude signal corresponding to the modified filtered output signal produced by the variable gain stage modifying the filtered output signal based on the digital gain code; generating a comparator output based on the amplitude signal and the DC reference voltage; and adjusting the digital gain code and the digital component code in combination until the comparator output indicates that the filter circuit is calibrated at the desired frequency; wherein adjusting the digital component code adjusts a combined value of the capacitive components in the filter circuit by selectively turning on or off one or more of the switches associated with the capacitive components to control a number of the capacitive

components active in the filter circuit to calibrate the filter circuit at the desired frequency." (Emphasis added). Thus, the claimed method recites initializing and adjusting a digital component code and a digital gain code in combination to calibrate a filter circuit to a desired frequency.

In contrast to claim 39, Douziech describes tuning the center frequency of a filter by toggling back and forth between two stored frequencies F1 and F2. (See Douziech at column 3, lines 6-54 and FIG. 1). As described in the previous response, Douziech does not generate the claimed digital component code and the digital gain code to tune the filter. Rather, Douziech describes using an **analog** tuning control signal 27 to tune the filter. Douziech generates the analog tuning control signal 27 by summing different analog signals output from corresponding analog components: the comparator 16, the switches 15 and 14, and filter tuning signal generator 20. In fact, FIG. 3 of Douziech illustrates the analog tuning control signal 27 as an analog filter tuning voltage that varies with different stored values (S1 and S2) of the filter amplitude.

While Douziech mentions "[a]nother embodiment [that] includes using digital techniques and/or software associated with suitable interfaces such as analogue-to-digital and digital-to-analogue converters," Douziech is silent as to how the digital techniques may be used. Further, even if digital techniques can be used, Douziech still does not describe or suggest any of the claimed limitations required of the claimed digital component code.

For example, in Douziech, the analog tuning control signal 27 is an analog voltage that changes to increase the center frequency of filter 11 to be closer to the frequency of the RF input signal 10. (See id. at col. 3, lines 64-66). However, Douziech is silent as to how the analog voltage increases the center frequency of the filter. Further, Douziech does not describe that the analog voltage is in any way associated with any component of the filter 11. Thus, generating the analog tuning control signal 27 in Douziech cannot reasonably be construed as the claimed "digital component code corresponding to switches associated with the capacitive components in the filter circuit based on the comparator output."

Moreover, the analog tuning control signal 27 in Douziech is a single analog signal fed to the filter. Douziech does not describe or suggest initializing the digital component code or initializing the digital gain code. Because Douziech fails to teach or suggest performing the initializations, Douziech also fails to teach or suggest adjusting the digital component code and the digital gain code in combination to calibrate the filter at the desired frequency as recited in claim 39.

The deficiencies of Douziech may be attributed to the innate difference between the device associated with the claimed method and the device described in Douziech. The claimed method is associated with a filter calibration circuit that consists of a DC voltage source, an amplitude detector; a comparator; and a calibration logic unit. The uncomplicated structure of the calibration circuit allows for a space saving design and more efficient calibration technique. In contrast to claim 39, Douziech requires extraneous components such as sample storages 21 and 22, a timing generator 17 and a summing terminal 24 as shown in FIG. 1. In addition, the device in FIG. 4 of Douziech includes all of the components in FIG. 1 and an extra comparator 16 to provide automatic gain control. Douziech describes that the automatic gain control is used to keep the output amplitude at a constant level rather than to calibrate the filter at a desired frequency. (See Douziech at column 5, lines 10-35). Moreover, the device in FIG. 6 of Douziech includes even more complexity by adding a ramp generator 49, another summing terminal 53, capacitors C1 and C2, and switches 61 and 62.

The addition of Kim fails to cure the deficiencies of Douziech. The Office contends to add the teachings of Kim merely to suggest that Kim teaches a capacitor array. However, Kim fails to teach or suggest initializing and adjusting a digital component code and a digital gain code in combination to calibrate the filter circuit at the desired frequency as recited in claim 39.

For at least these reasons, claim 39 is patentable over the proposed combination of Douziech and Kim.

Rejections Under 35 U.S.C. § 103(a) Based on Johnson and Kim

Claims 1-7, 9, 11, 12, 16-26, 28, 30, 31, 35-38, 55-61, 63, 65, 66, 70-80, 82, 84, 85 and 89-92 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,766,150 to Johnson ("Johnson") in view of U.S. Patent No. 5,963,856 to Kim ("Kim"). While not agreeing with the rejections, claims have been amended to obviate the rejections. Also, claims 2, 11, 12, 30, 31, 56, 65, 66, 84 and 85 have been cancelled.

Claim 1 and its dependent claims

Claim 1 has been amended to recite "[a] filter calibration circuit, consisting of: a DC voltage source operable to produce a reference amplitude signal; an amplitude detector configured to receive an output signal from a variable gain stage and produce an amplitude signal, wherein the output signal from the variable gain stage is produced by modifying an amplitude of an output signal produced by a filter circuit, which comprises capacitive components to be calibrated to a desired frequency; a comparator operable to generate a comparator output based on the amplitude signal of the amplitude detector and the reference amplitude signal of the DC voltage source; and a calibration logic unit, separate from the comparator, operable to receive the comparator output, produce a digital gain code based on the comparator output to adjust a gain of the variable gain stage, and produce a digital component code corresponding to switches associated with the capacitive components in the filter circuit to be used by the filter circuit in adjusting a combined value of the capacitive components in the filter circuit by selectively turning on or off one or more of the switches associated with the capacitive components to control a number of the capacitive components active in the filter circuit to calibrate the filter circuit to the desired frequency." (Emphasis added).

Thus, the claimed filter calibration circuit consists of a DC voltage source, an amplitude detector; a comparator; and a calibration logic unit. The uncomplicated structure of the claimed calibration circuit allows for an efficient and space saving design. In contrast to claim 39, Johnson requires extraneous components such as a D/A converter 370, an A/D converter 360, a crystal oscillator 305, a RF mixer 350 and a narrow band filter.

The addition of Kim fails to cure the deficiencies of Johnson. As described above, the Office contends to add the teachings of Kim merely to suggest that Kim teaches a capacitor array. However, Kim fails to teach or suggest the claimed filter calibration circuit that consists of a DC voltage source, an amplitude detector; a comparator; and a calibration logic unit.

For at least these reasons, claim 1 is patentable over the proposed combination of Johnson and Kim. Claims 3-7, 9 and 16-19 depend from claim 1 and are allowable for at least the same reasons.

Claim 20 and its dependent claims

Claim 20 is patentable over the proposed combination of Johnson and Kim for at least reasons similar to claim 1. Claims 20, 22-26, 28 and 35-38 depend from claim 1 and are patentable over the proposed combination for at least the same reasons.

Claim 55 and its dependent claims

Claim 55 is patentable over the proposed combination of Johnson and Kim for at least reasons similar to claim 1. Claims 57-61, 63 and 70-73 depend from clam 55 and are patentable over the proposed combination of Johnson and Kim for at least the same reasons.

Claim 74 and its dependent claims

Claim 74 is patentable over the proposed combination of Johnson and Kim for at least reasons similar to claim 1. Claims 76-80, 82 and 89-92 depend from claim 74 and are patentable over the proposed combination over Johnson and Kim for at least the same reasons.

Rejections Under 35 U.S.C. § 103(a) Based on Johnson, Kim and Miyazaki

Claims 93, 94, 96 and 97 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,766,150 to Johnson ("Johnson") in view of U.S. Patent No. 5,963,856 to Kim ("Kim") and further in view of US Patent No. 5,081,713 to Miyazaki ("Miyazaki"). While not agreeing with the rejections, the claims have been amended to obviate the rejections.

Claims 93, 94 and 96-97 have been incorporated into independent claims 1, 20, 55 and 74. Claims 1, 20, 55 and 74 are patentable over the proposed combination of Johnson and Kim as describe above. The addition of Miyazaki fails to cure the deficiencies of Johnson and Kim.

In contrast to claims 1, 20, 55 and 74, Miyazaki fails to teach of suggest the claimed filter calibration circuit that consists of a DC voltage source, an amplitude detector; a comparator; and a calibration logic unit. Similar to Johnson and Kim, the radio transmitter in Miyazaki requires extraneous components, such as a switch 21, temperature detector 22, reference voltage controller 22, a reference voltage generator 27, a power controller 18, a transmission frequency controller 24, a receiving section 25, and a transmission signal generating circuit 26. The added complexity in Miyazaki may be attributed to the requirement in Miyazaki to produce a reference voltage control signal with reference to a temperature characteristic of a detector for detecting the output signal (see Miyazaki at Abstract).

For at least these reasons, claims 1, 20, 55 and 74 are patentable over the proposed combination of Johnson, Kim and Miyazaki.

Rejections Under 35 U.S.C. § 103(a) Based on Johnson, Kim and Gabara

Claims 39, 40, 42, 44, 46, 47, 51-54 and 95 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,766,150 to Johnson ("Johnson") in view of U.S. Patent No. 5,963,856 to Kim ("Kim") and further in view of US Patent No. 6,307,443 to Gabara ("Gabara"). While not agreeing with the rejections, claims have been amended to obviate the rejections. Also, claims 40, 46, 47 and 95 have been cancelled.

Claim 39 and its dependent claims

As described above, claim 39 recites "initializing a digital component code…;" "initializing a digital gain code to a value such that a modified filtered output signal produced by a variable gain stage modifying the filtered output signal based on the initialized digital gain code is greater than a DC reference voltage;" "producing an amplitude signal…;" "generating a comparator output…;" and "adjusting the digital component code and the digital gain code in combination…" By initializing the digital component code and the digital gain code, the claimed method provides an optimal starting point to incrementally adjust the digital component code and the digital gain code in combination to calibrate the filter circuit at the desired frequency (e.g., the center frequency).

In contrast to claim 1, Johnson tunes a filter by using a filter calibration controller that stores reference signal levels corresponding to various transmit frequencies in its internal software and compares the level of the narrowband cavity filter output signal with the stored levels. (See id. at col. 8, lines 23-25; col. 9, lines 35-39). In Johnson, the filter is tuned until the measured value of the output signal level reaches a minimum, which indicates that the filter has been properly tuned to the center transmit frequency for the selected channel. (Col. 9, lines 62-65; col. 10, lines 12-14). Thus, the control signal that tunes the filter in Johnson is based on a comparison of an output signal against several stored reference signal levels.

Johnson does not describing using a digital component code and a digital gain code as recited in claim 39. For example, Johnson does not describe or suggest initializing a digital component code and a digital gain code as recited in claim 39. Moreover, Johnson does not describe or suggest adjusting the digital gain code and the digital component code in combination to calibrate the filter circuit at the desired frequency. This is not surprising because Johnson merely compares the output signal level against stored values. There is no need to calibrate a digital component code and a digital gain code in Johnson because Johnson does not adjust the two digital codes in combination to calibrate the filter.

The addition of Kim fails to alleviate the deficiencies of Johnson. As described above, Kim is cited by the Office to merely contend that Kim teaches an array of capacitive elements. Similar to Johnson, Kim fails to initialize and adjust the claimed digital component code and the digital gain code in combination to calibrate a filter circuit.

Also, Gabara fails to cure the deficiencies of Johnson and Kim. As described in the previous response, Gabara describes a bandpass filter with automatic tuning adjustment. (See Gabara at Abstract). To tune the filter in Gabara, a tuning signal is generated based on a comparison of the present power magnitude value to the previously-measured power magnitude. (See id. at col. 3, lines 13-17). Then, Gabara adjusts the tuning signal until the power of the filter output signal is maximized, which indicates that the filter is tuned to its dominant frequency. (See id. at col. 3, lines 17-19; Abstract). Gabara does not describe initializing and adjusting a digital component code and the digital gain code in combination to calibrate a filter circuit

For at least these reasons, claim 39 is patentable over the proposed combination of Johnson, Kim and Gabara. Claims 42, 44 and 51-54 depend from claim 39 and are patentable for at least the same reasons.

New Claim 98

The newly added claim 98 depends from claim 39 and is allowable for at least the same reasons. In addition, the proposed combinations fails to teach or suggest at least the claimed "wherein adjusting the digital gain code and the digital component code in combination until the comparator output indicates that the filter circuit is calibrated at the desired frequency comprises: decrementing a value of the digital gain code from the initialized value until the comparator output indicates that the amplitude signal is less than the DC reference voltage; incrementing a value of the digital component code; returning to the decrementing of the value of the digital gain code when the comparator output indicates that the amplitude signal is greater than the reference voltage; and decrementing the value of the digital component code when the comparator output indicates that the amplitude is less than the reference voltage after the incrementing the value of the digital component code."

CONCLUSION

The foregoing comments made with respect to the positions taken by the Examiner are not to be construed as acquiescence with other positions of the Examiner that have not been explicitly contested. Accordingly, the above arguments for patentability of a claim should not be construed as implying that there are not other valid reasons for patentability of that claim or other claims.

Please apply the one-month extension of time fees and any other charges or credits, to Deposit Account No. 06-1050.

Respectfully submitted,

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